APPLICATION

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TITLE: INTEGRATED PHOTODEVICE AND WAVEGUIDE

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INTEGRATED PHOTODEVICE AND WAVEGUIDE

TECHNICAL FIELD

5   This application relates to waveguides integrated with

semiconductor devices.

BACKGROUND

       Light propagates in straight line paths known as rays.

10 Rays are refracted, reflected, and scattered at material

interfaces. In a dielectric waveguide, a high index core

is surrounded by a lower index cladding layer, rays are

confined in the high index core region by total internal

reflection at the core/cladding interface. The reflected

15 rays interfere with each other to form electromagnetic

field patterns within the guide. Modes of the guide refer

to field patterns that propagate in the core region without

dispersion, i.e. changing shape.

       For electrical detection of light in a waveguide, the

20 light needs to be absorbed in the detector material and the

photogenerated charge must be collected. To improve

detection efficiency, the absorbing material is typically

placed in contact with the waveguide in a configuration

known as evanescent coupling. The detector coupling

efficiency can be improved by including an intermediate matching layer between the waveguide core and the absorbing detector material. This configuration still suffers from scattering loss from the detector material and inefficient

5   coupling due to mode repulsion and guiding in the matching layer.

Performance limits of a photodetector device are given by the gain bandwidth product. A photodetector with high gain will have diminished frequency response or bandwidth,

10   and a fast photodetector will have reduced gain or signal. The speed of a photodectector is limited by the transit time of the slowest carriers across the detector's active region.

15   **DESCRIPTION OF THE DRAWINGS**

Figs. 1A, 2A, 3A, 4A, 5A, 6A, 7A, 8A, 8C, 9A, 10A, and 11A are cross-sectional views of a phototransistor and waveguide at various stages of fabrication;

Figs. 1B, 2B, 3B, 4B, 5B, 6B, 7B, 8B, 9B, 10B, and 11B

20   are top views of a phototransistor and waveguide at various stages of fabrication;

Figs. 12A and 12C are cross-sectional views of a photodiode and waveguide; and

Fig. 12B is a top view of a photodiode and waveguide.

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DESCRIPTION

An integrated system of a phototransistor or photodiode coupled with a waveguide provides a relatively

5 fast, compact integrated photodetector with gain. The phototransistor or photodiode can serve as an element in a logic circuit, switched by light. A high index waveguide integrated with a phototransistor or photodiode efficiently couples light into a lossy detector material. The light is

10 absorbed in the detector material, which confines the electron hole pairs to a small region within a base of the phototransistor or intrinsic region of a photodiode. This configuration reduces the area of the base or intrinsic region and allows for faster switching frequency.

15 Furthermore, it allows the emitter collector current to be amplified.

Isolating a detector active material from incident evanescent mode tail, i.e., a portion of a light mode not confined to the waveguide core, with a cladding material

20 having a low index of refraction reduces losses due to reflection and diffraction at the input to the detector region. Further, a dielectric beveled mirror steers the light mode guided through the waveguide core into the detector material, increasing the coupling efficiency into

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the high index, high loss detector material by increasing

the angle of incidence on the detector material.

Referring to the cross-sectional view illustrated in

Fig. 1A, a silicon-on-insulator (SOI) substrate 10 has a

5   thin silicon layer 12 on its top surface, disposed over a

buried silicon dioxide layer 14. Silicon layer 12 and

buried silicon dioxide layer 14 are provided on a wafer 16,

e.g., an 8-inch silicon wafer. Thin silicon layer 12 has a

thickness T_1 of, e.g., 0.5 microns (μm). Buried silicon

10   dioxide layer 14 has a thickness T_2 of, e.g., 0.3 μm. Thin

silicon layer 12 is the top layer of SOI substrate 10, as

shown in the top view of Fig. 1B.

Referring to Fig. 2A, a cross-sectional view, and to

Fig. 2B, a top view of SOI substrate 10, an attenuating

15   layer 18 is deposited over silicon layer 12. Attenuating

layer 18 is a lossy material, i.e., it is capable of

absorbing light. Attenuating layer 18 has an index of

refraction higher than that of silicon. Further, the

material forming attenuating layer 18 is compatible with

20   silicon, so that attenuating layer 18 will not delaminate

from silicon layer 12. Attenuating layer 18 is, for

example, a germanium layer. Attenuating layer 18 is

deposited by a deposition method such as chemical vapor

deposition (CVD). In the case of a germanium attenuating

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layer 18, the deposition can be performed with germane gas and a hydrogen carrier at 600°C. The germanium can be deposited in a CVD system such as the Epsilon® manufactured by ASM International or the Epi xP Centura® manufactured by

5   Applied Materials. Attenuating layer 18 has a thickness T_3 of, e.g., 0.1 μm.

Referring also to the cross-sectional view of Fig. 3A and top view of Fig. 3B, a photoresist pattern (not shown) is defined on attenuating layer 18. Portions of

10   attenuating layer 18 not covered by the photoresist are removed by dry etching, such as by a chlorine/hydrogen bromide chemistry. Removal of portions of attenuating layer 18 exposes portions of the underlying thin silicon layer 12. Subsequently, exposed portions of underlying

15   thin silicon layer 12 are removed by dry etching by using a chlorine/hydrogen bromide chemistry, to expose portions 22a, 22b of buried oxide layer 14. Etching back to buried oxide layer 14 helps to electrically and optically isolate the phototransistor to be formed with its base below

20   attenuating layer 18. After etching of attenuating layer 18, a mesa region 20 is defined by a portion of attenuating layer 18 and silicon layer 12 that is not removed by the etching. Mesa region 20 has a width W_1 of, e.g., 6 μm. The

minimum width W_1 is determined by the dimensions of a

phototransistor to be built in mesa region 20 (see below).

Referring to the cross-sectional view illustrated in

Fig. 4A and top view shown in Fig. 4B, an intermediate

5   cladding layer 24 is deposited over buried oxide layer 14

and mesa region 20.   Intermediate cladding layer 24 is, for

example, a silicon dioxide layer, deposited by a method

such as plasma enhanced chemical vapor deposition (PECVD).

As deposited, intermediate cladding layer 24 has a

10   thickness of, for example, 1 μm, and a relatively low

refractive index of, e.g., 1.5.   Intermediate cladding

layer 24 is planarized by chemical mechanical polishing so

that a top surface 25 is substantially flat.   After

polishing, intermediate cladding layer 24 has a thickness T_4

15   of, for example, 0.85 μm above buried oxide layer 14.

Thickness T_4 of intermediate cladding layer 24 is selected

so that it is equal to or thicker than an evanescent tail

of a mode to be transmitted along a waveguide constructed

over intermediate cladding layer 24 (see below).   The

20   evanescent tail of a mode is the portion of light rays

propagated in a waveguide core that exponentially decay

outside the waveguide core.

Referring also to the cross-sectional view illustrated

in Fig. 5A and the top view illustrated in Fig. 5B, a

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photoresist layer (not shown) is patterned over

intermediate cladding layer 24. The photoresist layer

defines an opening over mesa region 20. A portion of

intermediate cladding layer 24 exposed by the opening in

5   the photoresist layer is removed over mesa region 20 by dry

etching to form a cladding layer window 26. Cladding layer

window 26 is defined by a first sidewall 27a and a second

sidewall 27b formed by intermediate cladding layer 24 and a

top surface 27c of mesa region 20. The dry etching is done

10   with a gas mixture such as trifluoromethane/oxygen

(CHF_3/O_2). Cladding layer window 26 has a width W_2 of,

e.g., 5.5 μm. Cladding layer window 26 width W_2 is less

than mesa region 20 width W_1, thereby facilitating

photolithographic alignment of cladding layer window 26

15   over mesa region 20.

Referring to the cross-sectional view shown in Fig. 6A

and the top view shown in Fig. 6B, a waveguide layer 28 is

formed over intermediate cladding layer 24. Waveguide

layer 28 is, for example, a silicon nitride layer deposited

20   by, e.g., PECVD using precursors of silane and nitrogen.

Waveguide layer 28 has a relatively high index of

refraction, higher than that of intermediate cladding layer

24. Waveguide layer 28, therefore, has an index of

refraction greater than 1.5, and, in some embodiments,

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greater than 1.9. In use, the high contrast between waveguide layer's 28 relatively high index of refraction and intermediate cladding layer's 24 relatively low index of refraction helps to confine light transmitted through

5 waveguide layer 28. Further, waveguide layer 28 is optically transparent in the wavelength region at which the completed device is to operate, for example, optically transparent for light having a wavelength of 850 nm.

Waveguide layer 28 covers intermediate cladding layer

10 24 and mesa region 20, and has a thickness T_5 above intermediate cladding layer 24 of, e.g., 0.3 μm. A top surface 30 of waveguide layer 28 defines an angle ϕ, with angle ϕ extending between a line A in a plane of waveguide top surface 30 over intermediate cladding layer 24 and a

15 line B in a plane of waveguide top surface 30 over first sidewall 27a in cladding layer window 26. The slope of waveguide top surface 30 in cladding layer window 26 defines a beveled mirror 31. Angle ϕ is selected such that, in use, a mode traveling through waveguide layer 28

20 undergoes total internal reflection off beveled mirror 31 and is directed into thin silicon layer 12 through attenuating layer 18. A critical angle of incidence θ_C is defined as

$$\theta_C = \sin^{-1}(n_2/n_1)$$

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where n_1 = refractive index of medium through which light is propagated, e.g., waveguide layer 28 and n_2= refractive index of proximate medium, e.g., intermediate cladding layer 24. Angle ϕ is, for example, 25°. Then, any angle ϕ

5   greater than 25° would cause total internal reflection and propagated light would be confined to waveguide layer 28.

Referring to the cross-sectional view illustrated in Fig. 7A and top view illustrated in Fig. 7B, a photoresist layer (not shown) is deposited and patterned over waveguide

10   layer 28. Portions of waveguide layer 28 not covered by the photoresist are subsequently removed by, for example, a dry etch. In the case where waveguide layer 28 is a silicon nitride layer, the dry etch can be performed with a gas mixture such as difluoromethane/oxygen (CH_2F_2/O_2). A

15   portion of waveguide layer 28 covered by photoresist is not etched away, thereby forming a waveguide core 32. Waveguide core 32 has a width W_3 of, e.g., 0.3 μm. Waveguide core 32 extends over intermediate cladding layer 24 and is in contact with mesa region 20.

20   Waveguide core 32 thickness T_5 and width W_3 are determined by the mode type to be propagated through waveguide layer 28 during use.   For single mode propagation, these dimensions need to be below the cutoff for the first mode and above the cutoff for a second mode.

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Waveguide core thickness T_5 and width W_3 are considerably

smaller than the free-space wavelength of light, having a

maximum of about 0.35 μm.

Referring to cross-sectional side view in Fig. 8A, top

5 view in Fig. 8B, and cross-sectional slice view in Fig. 8C,

an emitter 34 and a collector 36 are formed in thin silicon

layer 12 proximate waveguide core 32. Emitter 34 and

collector 36 are formed by an ion implantation by

implanting through attenuating layer 18, using waveguide

10 core 32 as a mask. In the case of a p-type thin silicon

layer 12, n-type ions are implanted, e.g., phosphorus ions,

with a dose of 10E14 atoms/centimeter-squared (atoms/cm^2),

and an energy of 20 kilo-electron volts (keV), to form

emitter 34 and collector 36, each having a junction depth D_1

15 of, e.g., 0.3 μm. A lateral phototransistor 40 is thereby

formed, with an n-type emitter 34, a n-type collector 36,

and a p-type base 38, with the p-type base 38 defined by

thin silicon layer 12. P-type base 38 has a length L_1 of,

e.g., 5.5 μm.

20 As noted above in reference to Figs. 4A and 4B, the

thickness T_4 of intermediate cladding layer 24 is selected

so that intermediate cladding layer 24 is equal to or

thicker than an evanescent tail of a mode to be transmitted

along waveguide core 32 constructed over intermediate

cladding layer 24. Intermediate cladding layer 24 prevents

the evanescent tail from reaching attenuating layer 18 made

of a lossy attenuating material, and thin silicon layer 12,

a lossy detector material. This offset increases the speed

5 of phototransistor 40 by reducing the amount of background

noise and making the phototransistor 40 more robust.

Hindering the evanescent tail from reaching thin silicon

layer 12 reduces the amount of extraneous light reflected

from thin silicon layer 12, thereby reducing the amount of

10 light necessary to turn on the transistor, as well as

reducing the amount of scattered light, which can affect

other transistors.

Waveguide core 32 is offset from mesa region 20 by an

offset distance D_2. Offset distance D_2 is, for example, 0.3

15 μm. Offset distance D_2 reduces reflection and scatter from

the attenuating layer 18 and thin silicon layer 12.

Referring to the cross-sectional view shown in Fig. 9A

and the top view shown in Fig. 9B, a top cladding layer 50

is deposited over waveguide 32, intermediate cladding layer

20 24, and an exposed portion of attenuating layer 18. Top

cladding layer 50 is, for example, silicon dioxide

deposited by a process such as PECVD. As deposited, top

cladding layer 50 has a thickness over intermediate

cladding layer 24 of, e.g., 1 μm. Top cladding layer 50 is

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planarized by chemical mechanical polishing, resulting in a

top cladding layer 50 thickness T_6 of, for example, 0.85 μm

over intermediate cladding layer 24.

Referring to the cross-sectional view shown in Fig.

5   10A and the top view shown in Fig. 10B, a photoresist layer

(not shown) is deposited and patterned on a top surface 52

of top cladding layer 50. The photoresist layer defines

openings over emitter 34 and collector 36. Portions of top

cladding layer 50 exposed by the openings defined by the

10   photoresist layer are removed by, for example, dry etching

with a CHF_3/O_2 plasma. Removal of portions of top cladding

layer forms first contact hole 60 over emitter 34 and

second contact hole 62 over collector 36. First and second

contact holes 60, 62 have a width W_4 of, for example, 0.2-

15   0.3 μm, and a depth D_3 of, for example, 0.85 μm. After the

etch, the photoresist layer is stripped.

Referring to the cross-sectional view illustrated in

Fig. 11A and the top view shown in Fig. 11B, an adhesion

layer 70 is deposited by CVD in a bottom portion of first

20   contact hole 60 and second contact hole 62. Adhesion layer

70 is a material such as titanium nitride, a material that

provides good adhesion and low contact resistance.

Subsequently, a metal 72 is deposited over adhesion layer

70 in first and second contact holes 60, 62. Metal 72 is,

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for example, tungsten deposited by CVD. Excess metal 72 is removed from top surface 52 of top cladding layer 50 by polishing. No metal contact is made to base 38 of phototransistor 40. Base 38, therefore, is left floating.

5   In use, attenuating layer 18 attenuates a mode propagated by waveguide core 32, and efficiently couples light into thin silicon layer 12 at base 38. Thin silicon layer 12 is a lossy detector, and defines a multimode cavity under mesa region 20. Attenuating layer 18 is also

10 a lossy material that absorbs light well. In the case where attenuating layer 18 is made of germanium, it has an extinction coefficient of about 40 times that of silicon, the extinction coefficient being the fraction of light lost to scattering and absorption. Attenuating layer 18,

15 thereby, contributes to the reduction of the length L_1 of the base region 38 needed to absorb and confine light propagated by waveguide core 32.

     The efficient coupling of a mode propagating through waveguide core 32 to base 38, therefore, reduces the

20 required length L_1 of base 38. The efficiency of the coupling is also improved both by the offset distance D_2 of waveguide core 32 from thin silicon layer 12 and by the steering of the mode into base 38 by beveled mirror 31. Beveled mirror 31 confines the mode in the waveguide core

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32 and directs the mode towards base 38. The buried oxide layer 14 beneath phototransistor 40 helps to confine light in the base region of phototransistor 40.

During operation, phototransistor 40 amplifies the induced photocurrent. Light transmitted by waveguide core 32 is absorbed in base 38, creating electron-hole pairs. Collector 36 has a positive bias, and photogenerated electrons in base 38 are therefore swept into collector 36. As holes are generated in base 38, the electrons are prevented from traversing base 38 and entering emitter 34. These holes charge base 38 proximate emitter 34, thus lowering the emitter-base barrier, i.e. lowering the barrier for electron emission from emitter 34 into base 38. Phototransistor 40 is thereby switched on with a large current between emitter 34 – collector 36, and the measured photocurrent is effectively amplified. The emitter 34/ collector 36 current is equal to the induced photocurrent times the gain of phototransistor 40. The relatively small base 38 and emitter 34 sizes result in fast response times.

In an alternative embodiment, referring to cross-sectional side view in Fig. 12A, top view in Fig. 12B, and cross-sectional slice view in Fig. 12C, SOI substrate 10 is processed as described above with reference to Figs. 1A – 7B. In this embodiment, thin silicon layer 12 is

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intrinsic, undoped silicon. An n-type region 100 and a p-type region 102 are formed in thin silicon layer 12 proximate waveguide core 32. N-type region 100 and p-type region 102 are formed by an ion implantation by implanting

5 through attenuating layer 18, using waveguide core 32 as a mask. Two separate photoresist masks (not shown) are used to separately define n-type region 100 and p-type region 102. To form n-type region 100, n-type ions are implanted, e.g., boron difluoride (BF_2), with a dose of 4x10E14

10 atoms/cm^2, and an energy of 30 keV. Also, p-type ions are implanted, e.g., phosphorus, with a dose of 4x10E14 atoms/cm^2, and an energy of 30 keV to form p-type region 102. Both n-type region 100 and p-type region 102 have a depth of D_4 of, e.g., 0.3 μm. A lateral p-i-n photodiode

15 104 is thereby formed, with n-type region 100, p-type region 102, and an intrinsic silicon region 106 between n-type region 100 and p-type region 102. SOI substrate 10 and lateral p-i-n photodiode 104 are processed further in the manner described with reference to Figs. 9A-11B.

20 This application is not limited to the specific embodiments described above. For example, the buried silicon dioxide layer 14 can have a thickness of up to several microns. A portion of the attenuating layer 18 can be removed by wet etching. A photodevice can be fabricated

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without attenuating layer 18. Thin layer 12 can be a material other than silicon, such as such as germanium. The portions of the thin silicon layer 12 proximate the mesa region 20 can be left unetched. The intermediate

5   cladding layer 24 can be thinner than the evanescent tail of a mode to be propagated through waveguide core 32. A portion of the cladding layer 24 can be removed by a wet etch, such as etching with hydrofluoric acid (HF) which etches oxides but does not attack germanium. Waveguide

10   layer 28 can be a material other than silicon nitride, such as silicon oxynitride. The emitter 34 and collector 36 can be implanted by using a photoresist mask. The emitter 34 and collector 36 can be implanted with other types of n-type ions, such as arsenic, with a dose of 10E14 atoms/cm^2,

15   and an energy of 80 – 100 keV. Alternatively, with an n-type thin silicon layer 12, the emitter 34 and collector 36 can be formed by the implantation of p-type dopants. A single photoresist layer can be used to define n-type 100 and p-type 102 regions in lateral p-i-n diode 104, with the

20   waveguide core 32 acting as a mask to protect intrinsic silicon region 106 from implantation. Top cladding layer 50 can be deposited by alternative deposition methods, such as by high-density plasma (HDP) deposition.